An *L*-Band Ultra-Low-Power-Consumption Monolithic Low-Noise Amplifier

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***Abstract*—A low-power-consumption variable-gain low-noise amplifier (LNA) is demonstrated. To achieve low noise, low distortion, and low power consumption simultaneously, a cascode connection between an enhancement-mode GaAs MESFET (EFET) and a depletion-mode GaAs MESFET (DFET) is employed. The EFET is superior to the DEFT in its gain and noise figure performance while the DFET offers good intermodulation distortion performance. The advantages of both types of FET's are combined in the developed LNA. It shows excellent performance with an NF of 2.0 dB, a gain of 12.2 dB, and an IP_3 of 5.1 dBm at 1.9 GHz. The demonstrated performance satisfies the specifications of the Japanese Personal Handy phone System even at the ultra-low power consumption of 2.0 mW.**

I. Introduction

IN MOBILE communication systems, it is important to extend the operation time and miniaturize the volume and weight of handy phone sets. To conserve the battery, low-current-operation circuit technologies are essential. Reducing battery size reduces the set's volume and weight. This is because the battery is the largest and heaviest single component in handy phone sets. However, when battery size is decreased, battery capacity is decreased proportionally. Therefore, if the current level of service is to be maintained, and hopefully expanded, circuits that can operate at low voltage and low current will be required [1]–[9].

Reducing the operation voltage of the digital circuits used in handy phone sets makes it possible to reduce their power consumption owing to the scaling effect. When it becomes possible to operate analog circuits at the same voltage as digital circuits use, it will be a big breakthrough towards decreasing total power consumption. Moreover, since no voltage adjusting circuit (e.g., a dc-dc voltage converter) is required, the circuit configuration becomes simpler.

LNA's need to achieve maximum performance at the lowest possible power consumption and a tradeoff exists among their noise figure (NF), third order intermodulation distortion (IM_3), and gain characteristics. This paper describes an ultra-low-power-consumption monolithic LNA which consumes only less than 1 mA at 2 V. It satisfies the desired specifications at very low power consumption.

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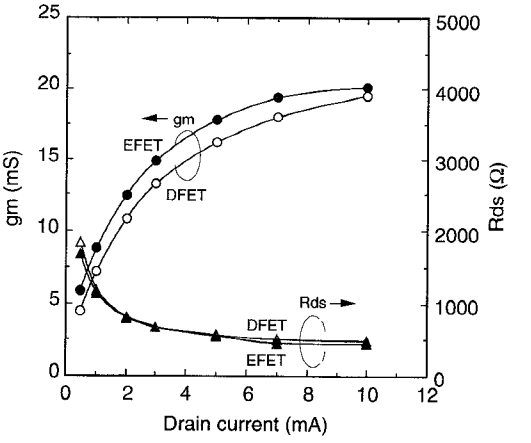

Fig. 1. EFET/DFET g_m and R_{ds}—drain current dependence.

II. EFET and DFET Characteristics

A. Fabrication and Measurement

EFET and DFET features were investigated by using dc and RF measurements. We compared them in terms of gain, NF, and IM_3 performances to determine which types of amplifiers they would be better suited for. The gate widths used in the experiments were 100 μm for both FET's. An EFET was fabricated with 30 keV and 4.0 $\times 10^{12}$ cm^{-2} Si implantation and a DFET with 30 keV and 11.2 $\times 10^{12}$ cm^{-2}. In this experiment, the same implantation energy was adopted to fabricate both FET's; only the dose was changed. This simplifies their fabrication process. Though process parameters are not always optimum in this case, it is effective in realizing a practical technique for mass cost-oriented production.

The g_m, R_{ds}, C_{gd} and maximum stable gain (MSG) of each FET, all of which were derived from RF measurements, are compared in Figs. 1 and 2. F_T and C_{gs} are compared in Fig. 3. All values are plotted as a function of drain current. EFET and DFET properties are discussed in the following sections.

B. Gain Characteristics

The EFET has inherently high transconductance g_m characteristics [9]. Fig. 4 shows g_m versus gate voltage V_g curves of the EFET and DFET obtained through dc measurement. The K-values is defined as

$$K = \Delta g_m / \Delta V_g.$$

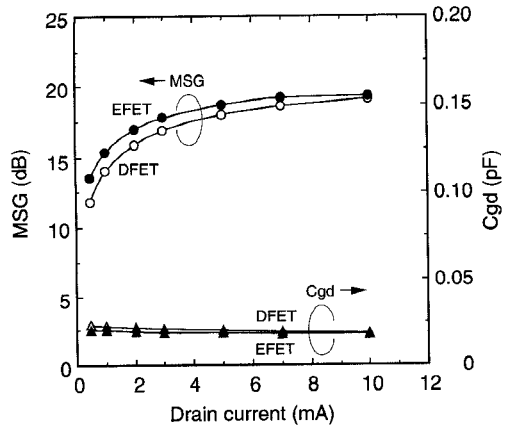

Fig. 2. EFET/DFET MSG and C_{gd}—drain current dependence.

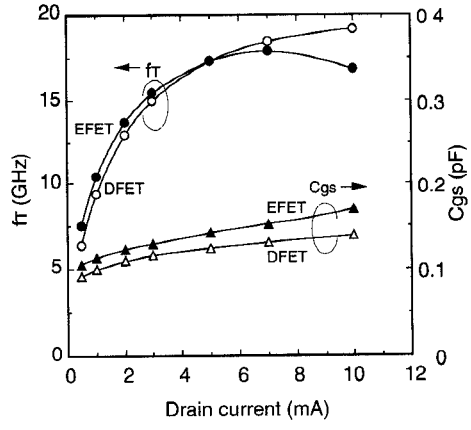

Fig. 3. EFET/DFET f_T and C_{gs}—drain current dependence.

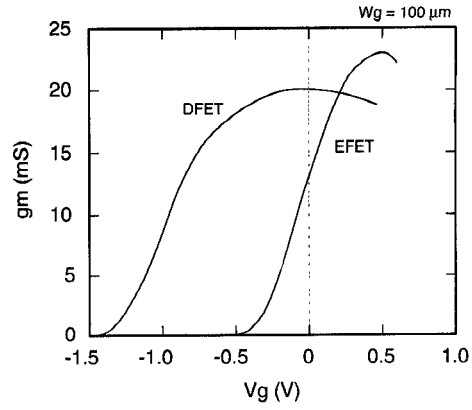

Fig. 4. EFET/DFET g_m-V_g characteristics.

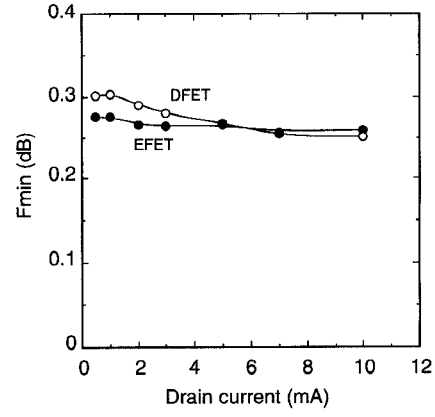

Fig. 5. EFET/DFET $F_{\min}$—drain current dependence.

This is a figure of merit for indicating the gradient of the g_m-V_g curve near the region where V_g equals V_{th}. The K-values of the EFET and DFET are 200 and 150 mS/Vmm, respectively, and the maximum g_m of the EFET and DFET are 230 and 200 mS/mm, respectively. The gradient of the g_m-V_g curve for the EFET is steeper than it is for the DFET.

The R_{ds} characteristics are almost equal, and the g_m of the EFET is larger than that of the DFET over the entire drain current range shown in Fig. 1. At 1 mA, the g_m of the EFET is 8.8 mS and that of the DFET is 7.2 mS. In Fig. 2, the MSG of the EFET is larger than that of the DFET at any current level, which is due to the large g_m characteristics of the EFET because C_{gd} characteristics are almost equal for both FET's.

According to the dc and RF measurements, the difference in gain performance between the EFET and DFET is mainly derived from their different g_m characteristics. Large g_m implies high gain characteristics. The EFET, therefore, has a higher gain than the DFET at the same current level.

C. NF Characteristics

Noise performance can, according to the equivalent circuit parameters, be predicted by Fukui's equation [10]

$$F_{\min} = 1 + 2\pi K_f \cdot f \cdot C_{gs}((R_s + R_g)/g_m)^{1/2}.$$

where $F_{\min}$ is the minimum noise figure, K_f is a fitting factor (approximately 2.5), and f is the operation frequency. As both FET's were fabricated with the same implantation energy, their profiles are quite similar and only their carrier concentration is different. Therefore, they can be compared using the same fitting factor.

$F_{\min}$ of the EFET and DFET were calculated using the above equation and plotted in Fig. 5. The $F_{\min}$ of the EFET is better than that of the DFET when the drain current is less than 5 mA. The difference in NF performance can be explained by the f_T, C_{gs} and g_m characteristics of the two FET's. The g_m of the EFET is larger than that of the DFET over the entire drain current level, and $R_g + R_s$ is almost equal for both FET's. Since the C_{gs} difference decreases as the drain current decreases, the contribution of g_m characteristics to $F_{\min}$ characteristics increases significantly. Though the C_{gs} of the EFET is larger than that of the DFET, the EFET's g_m is large enough to maintain its better f_T performance at low drain currents. As a result, the EFET has low NF characteristics owing to its higher f_T [11].

The C_{gs} characteristics shown in Fig. 6 are normalized by the value at 1 mA drain current to show clearly their current dependence. As the drain current increases above 5 mA, the C_{gs} of the EFET noticeably increases and this degrades the EFET's f_T and $F_{\min}$ performances under large drain current conditions. This is confirmed in Fig. 3; when the drain current is more than 5 mA, the f_T of the EFET peaks and start to decrease.

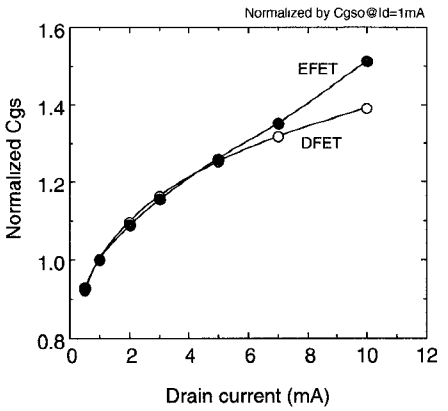

Fig. 6. EFET/DFET normalized C_{gs}—drain current dependence.

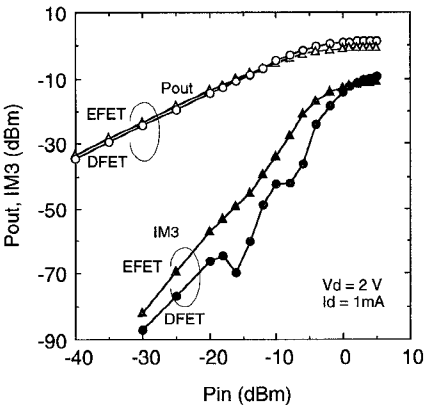

Fig. 8. EFET/DFET IM_3 characteristics.

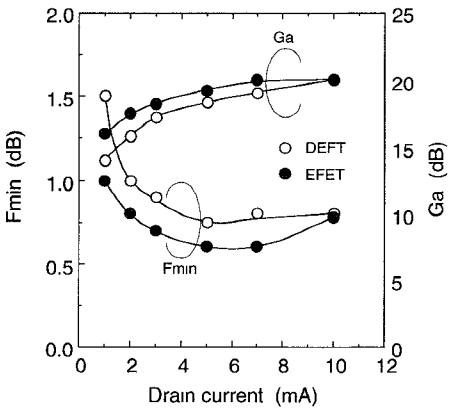

Fig. 7. EFET/DFET $F_{\min}$ and G_a—drain current dependence.

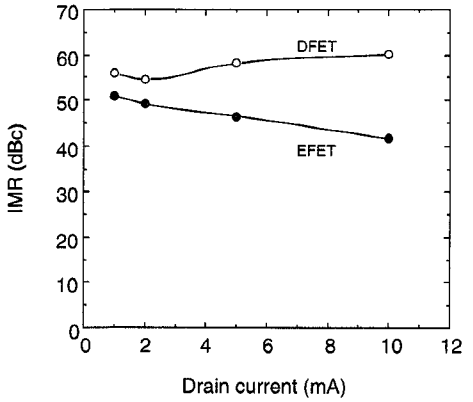

Fig. 9. EFET/DFET IMR—drain current dependence.

$F_{\min}$ and associated gain (G_a) of the EFET and DFET measured at 2 GHz are shown in Fig. 7. The EFET shows better $F_{\min}$ performance than the DFET. Its superiority over the DFET increases in the small drain current region.

Both $F_{\min}$ and f_T characteristics show that the EFET has better NF performance than the DFET, especially under low drain current conditions.

D. IM_3 Characteristics

IM_3 characteristics of the EFET and DFET are shown in Fig. 8. They were measured at the drain voltage of 2 V and current of 1 mA. Their input and output impedances were matched with slide screw tuners. As can be seen from the figure, the DFET offer better IM_3 performance. Fig. 9 shows the intermodulation distortion ratio (IMR) versus drain-current characteristics of the EFET and DFET, which were measured with -25 dBm input power and 2-V drain voltage. The DFET's IMR performance is better than that of the EFET at all drain current levels, and this advantage gradually improves as the current increases. On the other hand, the EFET's IMR performance degrades as the current is increased. Although the g_m of the DFET is smaller than that of the EFET, it changes less as V_g varies. Thus, the nonlinear effect attributable to the g_m characteristics of the DFET is less than that attributable to those of the EFET, and this results in the DFET's low distortion characteristics. The g_m of the DFET saturates at around V_g of 0 V, where the drain current is large. Here, the g_m nonlinear effect is much less than it is in a small drain current region. This explains why the IMR performance of the DFET is better in this case. In the EFET, the g_m nonlinear effect is larger than it is in the DFET, and the C_{gs} increases much more than it does in the DFET with an increase in the drain current, as shown in Fig. 6. In addition to the g_m effect, the nonlinear effect, which is due to C_{gs} characteristics, causes distortion in the EFET. Since the EFET's nonlinear effect caused by C_{gs} is significant in the large drain current region, its IMR performance worsens as the drain current is increased.

E. Summary of FET Performances

The gain, NF and IM_3 performances of the EFET and DFET are summarized in Table I. When multistage amplifiers are designed, the input side amplifiers are required to have high gain and low NF performance. Therefore, EFET's are suitable as input side amplifiers. For output side amplifiers, good IM_3 performance is needed because their input power is delivered from input side amplifiers, and they receive more power than the input side amplifiers. The good IM_3 performance of the DFET's makes them attractive for use as output side amplifiers.

TABLE I
SUMMARY OF THE EFET AND DFET PERFORMANCE

	EFET	DFET
Gain	Excellent	Good
NF	Excellent	Good
IM3	Fair	Excellent

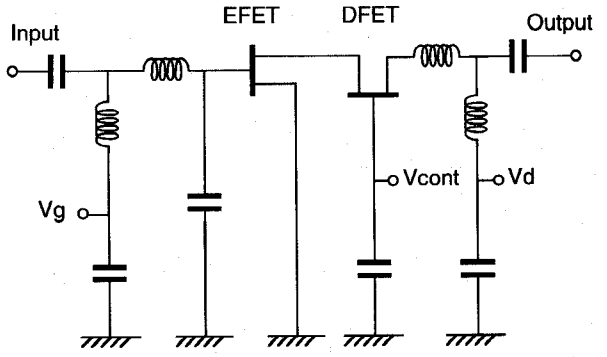

Fig. 10. LNA schematic circuit.

III. CIRCUIT DESIGN

The key to optimizing the RF circuits used in handy phone sets is reducing their power consumption. In order to meet the gain requirement, multistage amplifiers, usually two stages, are adopted. Since every stage of amplifier consumes certain amount of the drain current, the total current consumption is increased in proportion to the number of the stages. When only one current flows through all stages of the amplifiers, the total current consumption is reduced to the one amplifier current consumption [12]. The cascode amplifier can be regarded as two-stage amplifier and the current is fed to a common gate FET through a common source FET by the same bias line. Moreover, it has high output power capability [13], [14]. Thus, the cascode amplifier was chosen as the basic configuration of the high gain and low power consumption amplifier.

The developed LNA employs a cascode connection between an EFET and a DFET as shown in Fig. 10. When the EFET's high gain and low NF characteristics are suitably combined with the DFET's excellent IM_3 performance, it will contribute greatly to the development of an LNA which operates at a reduced current level. The cascode-connection LNA has the advantages of high gain and variable control. The gain is increased, NF and IMR performance are improved when using an EFET as a common source FET and a DFET as a common gate FET in the cascode connection [6].

Both of these FET's were fabricated at the same time by using a type of selected ion implantation process (SAINT process [15]). They have a buried p-layer, and are characterized by high K-values and low knee-voltage. Therefore, these devices have a lot of advantages in achieving low-power-consumption and high-performance LNA's.

The loss of the input matching circuit degrades LNA's NF performance and its gain performance is degraded by the total loss of the matching circuits. In order to offset these losses, low loss inductors, which are wide-line-width and thick-metal, were incorporated into the matching circuits of the LNA. The line-width is 20 μm and the metal-thickness is 4.2 μm. These inductors have less than one-eighth the parasitic resistance of our previously developed conventional ones.

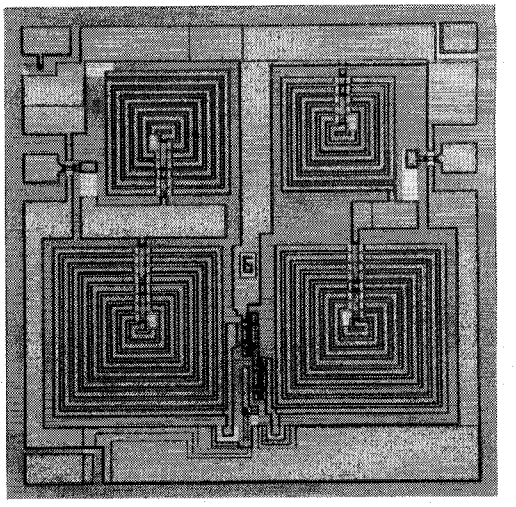

Fig. 11. LNA photograph.

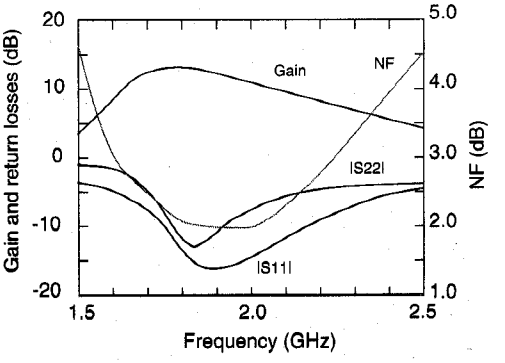

Fig. 12. LNA small signal and NF performance.

The threshold voltages of the EFET and DFET were -0.1 V and -1.0 V, respectively, and W_g and L_g were 100 μm and 0.3 μm for both devices. Lumped elements, such as MIM capacitors and spiral inductors, were adopted for input and output matching circuits to reduce the LNA chip size [1].

IV. RESULTS AND DISCUSSION

A photograph of the LNA is shown in Fig. 11. Chip size was 1.3 mm $\times$ 1.3 mm.

Gain, return losses, and NF characteristics measured at 2.0 V and 1 mA are shown in Fig. 12. The performances obtained at 1.9 GHz were 12.2 dB gain, 16.2 dB input return loss, 11.1 dB output return loss, and 2.0 dB NF.

Variable gain performance of the LNA is shown in Fig. 13. The gain can be controlled to match the system requirement and can be held to less than 0 dB by controlling the gate voltage of the common gate FET. Moreover, the LNA can be fully turned off by applying a large negative control voltage, i.e. less than -1.4 V.

The IM_3 characteristics of the LNA are shown in Fig. 14. The IMR measured at the power input of -30 dBm was 47 dBc, and the IP_3 was 5.1 dBm.

The supplied voltage dependencies are shown in Fig. 15. The gain and NF are almost the same at any supplied voltage.

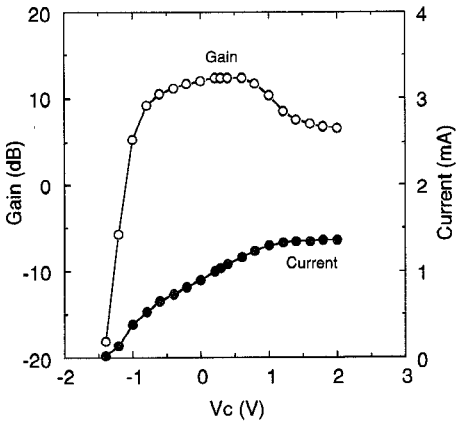

Fig. 13. LNA gain controllability.

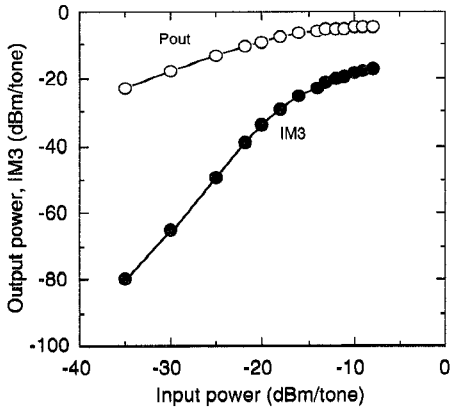

Fig. 14. LNA IM_3 characteristics at 2 V and 1 mA.

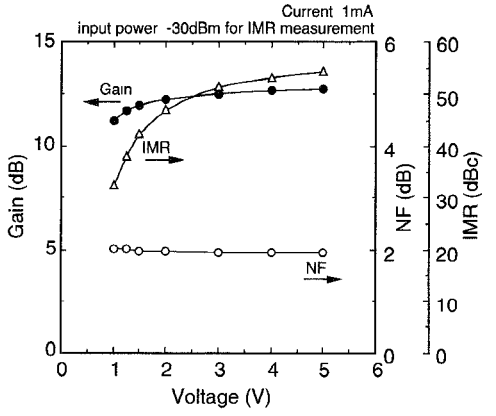

Fig. 15. LNA gain, NF, and IMR—supplied voltage dependence.

The IMR performance is dependant on voltage, however adequate IMR values are achieved at approximately 2 V and beyond.

In order to confirm our design strategy, we fabricated two other cascode connection LNA's: the first, the D/D LNA, employed DFET's as both the common source and the common gate FET; the second, the E/E LNA, employed only EFET's. All LNA's had the same equivalent circuit. Characteristics were measured as a function of drain current at the constant drain voltage of 2.0 V.

Gain and NF characteristics for the E/D and D/D LNA's are compared in Fig. 16. The E/D LNA gain is larger than that

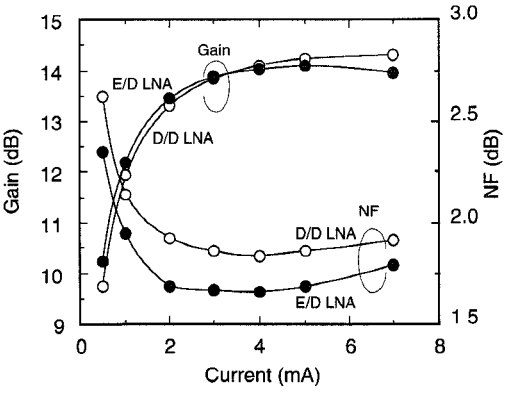

Fig. 16. Gain/NF comparison—E/D LNA versus D/D LNA.

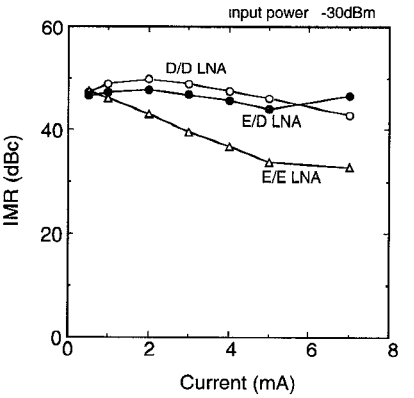

Fig. 17. IMR comparison—E/D, D/D, and E/E LNA.

of the D/D in the region below 3.0 mA, and the E/D LNA NF is smaller than that of the D/D for all measured current levels. These results show the superiority of the E/D LNA over the D/D in gain and NF performance, especially under low current conditions.

Fig. 17 compares the IMR characteristics of all three LNA's. The E/E LNA has worse IMR performance than other two LNA's. The E/D and D/D LNA offer almost the same performance. These are attributable to the good IMR characteristics of the DFET. The E/D LNA achieves the required gain, NF, and IMR performance because it offers higher gain than D/D without IMR degradation.

We compared the new LNA to previously reported MMIC LNA's and the results are shown in Fig. 18. Here, the vertical axis is the receiver NF, which is the total NF assuming the connection of a 10-dB NF circuit (e.g., a mixer) to the LNA output. We introduced this value to compare gain, NF, and power consumption simultaneously. As can be seen in Fig. 15, the LNA reported in this paper achieves the best overall performance among all LNA's reported to date.

V. Conclusion

An *L*-band ultra low power consumption monolithic LNA has been demonstrated. The LNA uses an EFET and DFET in cascode connection to achieve low noise, low distortion, and low power consumption simultaneously. It can operate with a supplied voltage of 2 V and its power consumption is less than 2 mW. Optimal performance is achieved with an a NF of 2.0 dB, a gain of 12.2 dB, and an IP_3 of 5.1 dBm at

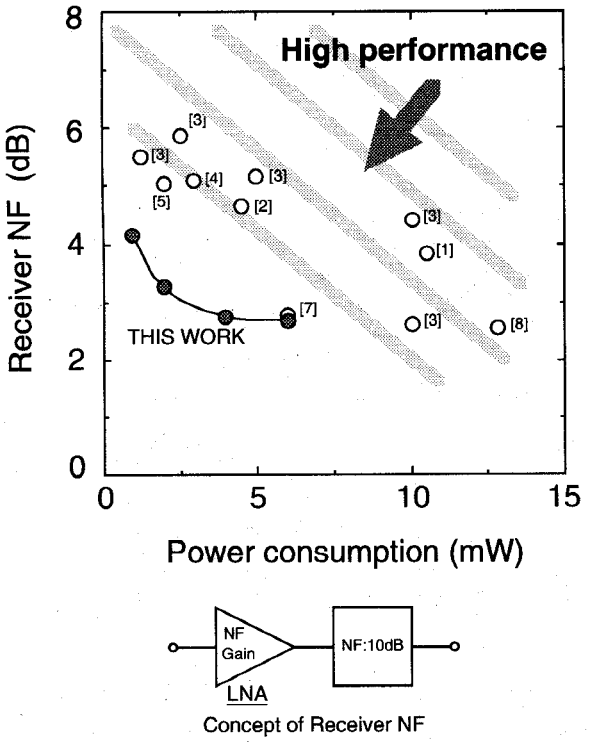

Fig. 18. Comparison of this work with previously reported LNA's.

1.9 GHz. Its demonstrated performance will make it suitable for application in the Japanese Personal Handy phone System (PHS). This LNA is one of the most promising devices yet developed to reduce battery size for mobile communication equipment.

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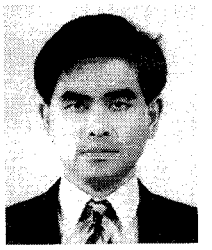

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